IN THE CLAIMS

Per the revised amendment practice, a complete listing of all claims in the application follows.

1. (Original) A method of establishing electrical communication between a first device and a second device in a semiconductor circuit, comprising:

contacting said first device with a first end of an electrically conductive material;

layering an initial barrier component over a second end of said electrically conductive material;

nitridizing at least a portion of said initial barrier component; and

contacting said second device with said portion of said initial barrier component.

2. (Original) The method in claim 1, further comprising a step of siliciding at least a second portion said initial barrier component.

3. (Original) The method in claim 2, wherein said step of contacting said first device further comprises contacting a transistor with doped silicon; and wherein said step of contacting said second device further comprises contacting a capacitor.

4. (Original) The method in claim 3, wherein said step of contacting said second device further comprises contacting a capacitor with a doped polysilicon plug.

5. (Original) A method of processing a semiconductor circuit on a substrate covered with an insulating layer, wherein said layer defines an opening over said substrate, and polysilicon contacts a surface of said substrate and a bottom of said opening; and wherein said method comprises:

providing an initial barrier component on at least said polysilicon; and

nitridizing said initial barrier component.

6. (Original) The method in claim 5, further comprising siliciding said initial barrier component.

7. (Original) The method in claim 6, further comprising a step of providing an oxidation protection layer within said opening.

8. (Original) The method in claim 7, further comprising a step of recessing said polysilicon.

9. (Original) The method in claim 8, wherein said step of providing an initial barrier component further comprises providing said initial barrier component only on said polysilicon.

10. (Original) The method in claim 9, wherein said step of providing said initial barrier component comprises depositing said initial barrier component through selective chemical vapor deposition.

11. (Currently amended) The method in claim ~~9~~ 8, wherein said step of providing said initial barrier component further comprises the steps of:

depositing said initial barrier component on said polysilicon and within said opening; and

etching said initial barrier component within said opening.

12. (Original) A method of preparing a semiconductor device comprising a container defined by at least one insulation layer, comprising:

forming a poly plug extending toward said container and having a surface under said container;

depositing an initial barrier component at least between said poly plug and said container; and

nitridizing a first portion of said initial barrier component, wherein said first portion is next to said container.

13. (Original) The method in claim 12, further comprising a step of siliciding a second portion of said initial barrier component, wherein said second portion is between said poly plug and said first portion of said initial barrier component.

14. (Original) The method in claim 13, further comprising a step of depositing an oxidation protection layer within said container and over said first portion.

15. (Original) The method in claim 14, wherein said step of depositing an initial barrier component further comprises lining said container with said initial barrier component; and wherein said step of nitridizing a first portion of said initial barrier component further comprises nitridizing said initial barrier component lining said container.

16. (Original) A method of forming an interface between a transistor and a capacitor, wherein said transistor includes a doped portion of a substrate, and an in-process poly plug is supported by said doped portion and extends upward along a length to a capacitor site, and wherein said method comprises:

reducing said poly plug to generally half of said length;

selectively chemically vapor depositing a barrier component onto said poly plug, wherein said barrier component has a bottom next to said poly plug and a top opposite from said bottom; and

nitridizing said top of said barrier component.

17. (Original) The method in claim 16, wherein said step of nitridizing further comprises nitridizing generally half of said barrier component.

18. (Original) The method in claim 17, further comprising a step of siliciding said bottom of said barrier component.

19. (Original) The method in claim 18, wherein said step of siliciding further comprises siliciding generally half of said barrier component.

20. (Currently amended) A method of interfacing a silicon contact with a semiconductor device, comprising:

forming a barrier to diffusion from said silicon contact using a first material layered

over said silicon contact; and

forming a barrier to oxidation of said silicon contact using a selection of said first material and a second material, wherein said barrier to oxidation is discrete from said semiconductor device.

21. (Original) The method in claim 20, wherein said step of forming a barrier to oxidation further comprises providing a layer of ruthenium oxide.

22. (Original) The method in claim 20, wherein said step of forming a barrier to diffusion further comprises layering over said silicon contact a selection of platinum, iridium, osmium, palladium, rhodium, ruthenium, and oxides thereof; and wherein said step of forming a barrier to oxidation further comprises forming a barrier to oxidation using said selection.

23. (Currently amended) The method in claim 20, wherein said step of forming a barrier to diffusion further comprises providing a metal nitride layer; and wherein said step of forming a barrier to oxidation further comprises providing a layer ~~comprised~~ consisting of a selection of a metal or a metal oxide.

24. (Original) The method in claim 23, wherein:

said step of forming a barrier to diffusion further comprises providing a first layer selected from:

a nitride of titanium, tungsten, rhenium, and platinum-group metals,

an oxide of said platinum-group metals,

an alloy of said platinum-group metals, and

a boride of a transition metal; and

said step of forming a barrier to oxidation further comprises providing a second layer over said first layer, wherein said second layer is selected from platinum-group metals and an oxide of platinum-group metals.

25. (Currently amended) A method of establishing electrical contact between a semiconductor substrate and a semiconductor device, comprising:

covering said substrate with an insulating layer;

etching a hole through said insulating layer to said substrate;

partially plugging said hole with doped polycrystalline silicon;

selectively depositing at least one metal layer within said hole over said doped polycrystalline silicon;

nitridizing said at least one metal layer;

siliciding said at least one metal layer; and

forming said semiconductor device over said at least one metal layer.

26. (Original) The method in claim 25, wherein:

said step of depositing at least one metal layer comprises depositing a titanium layer;

said step of nitridizing said at least one metal layer comprises nitridizing said titanium layer; and

said step of siliciding said at least one metal layer comprises siliciding said titanium layer.

27. (Currently amended) ~~The method in claim 25, wherein:~~ A method of establishing electrical contact between a semiconductor substrate and a semiconductor device, comprising:

covering said substrate with an insulating layer;

etching a hole through said insulating layer to said substrate;

partially plugging said hole with doped polycrystalline silicon;

depositing at least one metal layer within said hole over said doped polycrystalline silicon;

siliciding said at least one metal layer, wherein said step of siliciding said at least one metal layer comprises siliciding a titanium layer;

nitridizing said at least one metal layer, wherein said step of nitridizing said at least one metal layer comprises nitridizing a non-titanium layer; and

forming said semiconductor device over said at least one metal layer, wherein said step of forming said semiconductor device further comprises forming said semiconductor device over said non-titanium layer.

Claim 28 (cancelled).

29. (Currently amended) A damascene process, comprising:

forming a first insulation layer over a semiconductor substrate;

forming a first hole in said first insulation layer;

forming doped polysilicon in said first hole; ~~and~~

selectively depositing a material over said doped polysilicon; and

forming a silicon barrier from said material ~~over said doped polysilicon~~.

30. (Currently amended) The process in claim 29, wherein said step of forming doped polysilicon further comprises forming doped polysilicon having a ~~low~~ surface within said first hole that is lower than a top of said first insulation layer.

31. (Currently amended) The process in claim 30, wherein said step of forming doped polysilicon having a ~~low~~ surface within said first hole further comprises:

generally completely filling said first hole with said doped polysilicon; and

etching a portion of said doped polysilicon.

32. (Original) The process in claim 31, further comprising a step of forming an oxygen barrier over said silicon barrier.

33. (Original) The process in claim 32, further comprising a step of forming an electrical contact enhancement layer under said silicon barrier.

34. (Currently amended) ~~The process in claim 33, further comprising:~~ A damascene process, comprising:

forming a first insulation layer over a semiconductor substrate;

forming a first hole in said first insulation layer;

forming doped polysilicon in said first hole, wherein said step of forming doped

polysilicon further comprises forming doped polysilicon having a low surface within said first hole, wherein said step of forming doped polysilicon having a low surface within said first hole further comprises:

generally completely filling said first hole with said doped polysilicon, and

etching a portion of said doped polysilicon;

forming a silicon barrier over said doped polysilicon;

forming an oxygen barrier over said silicon barrier;

forming an electrical contact enhancement layer under said silicon barrier;

forming a second insulation layer over said first insulation layer; and

forming a second hole in said second insulation layer, wherein said second hole is over said first hole.

35. (Original) The process in claim 34, wherein said step of forming an oxygen barrier further comprises forming an oxygen barrier extending into said second hole.

36. (Currently amended) A method of processing a semiconductor device, comprising:

providing ~~an~~ silicon interconnect material contacting an electrically conductive first portion of said semiconductor device; and

selectively providing an initial barrier component ~~contacting~~ on said interconnect material.

37. (Original) The method in claim 36, wherein said step of providing an initial barrier component further comprises initially protecting said semiconductor device against silicon diffusion.

38. (Original) The method in claim 36, wherein said step of providing an initial barrier component further comprises initially providing a component capable of protecting said semiconductor device against silicon diffusion after further processing.

39. (Currently amended) ~~The method in claim 38, further comprising~~ A method of processing a semiconductor device, comprising:

providing a silicon interconnect material contacting an electrically conductive first portion of said semiconductor device;

providing an initial barrier component contacting said interconnect material, wherein said step of providing an initial barrier component further comprises initially providing a component capable of protecting said semiconductor device against silicon diffusion after further processing; and

nitridizing said initial barrier component; and wherein said step of initially providing a component further comprises providing a component capable of protecting said semiconductor device against silicon diffusion after being nitridized.

40. (Original) A method of preventing at least some diffusion from a conductive material in a semiconductor device, comprising:

surrounding a side of said conductive material with an insulator;

depositing a barrier material onto said conductive material; and

nitridizing said barrier material.

41. (Original) The method in claim 40, wherein said step of depositing a barrier material further comprises depositing said barrier material onto said conductive material and onto said insulator.

42. (Original) The method in claim 41, further comprising a step of removing said barrier material from said insulator.

43. (Currently amended) A method of treating a silicon contact, comprising:

depositing a barrier component selectively onto said silicon contact; and

nitridizing said barrier component.

44. (Original) The method in claim 43, wherein said step of depositing a barrier component further comprises siliciding said barrier component.

45. (Currently amended) ~~The method in claim 43, further comprising a step of~~ A method of treating a silicon contact, comprising:

depositing a barrier component onto said silicon contact;

nitridizing said barrier component; and

discretely siliciding said barrier component.

46. (Original) The method in claim 45, wherein said step of discretely siliciding said barrier component further comprises siliciding at least an un-nitridized portion of said barrier component.

47. (Original) The method in claim 46, wherein said step of discretely siliciding said barrier component further comprises reacting said barrier component with silicon in said silicon contact.

48. (Currently amended) The method in claim 47, wherein said step of reacting said barrier component further comprises reacting said barrier component with a portion of said silicon contact containing at least one oxygen atom.

49. (Currently amended) A memory cell, comprising:

a transistor;

a capacitor;

a silicon plug extending from said transistor toward said capacitor and physically separate from said capacitor; ~~and~~

a diffusion barrier between said silicon plug and said capacitor; and

a contact enhancer physically integral to said diffusion barrier.

50. (Original) The memory cell in claim 49, wherein said diffusion barrier is made of a metal nitride.

51. (Original) The memory cell in claim 50, wherein said diffusion barrier is made of titanium nitride.

52. (Currently amended) The memory cell in claim 51, ~~further comprising~~ wherein said contact enhancer comprises an un-nitridized ~~layer~~ portion of titanium between said diffusion barrier and said silicon plug.

53. (Currently amended) The memory cell in claim 52, wherein said un-nitridized ~~layer~~ portion of titanium is a silicided layer of titanium.

54. (Currently amended) ~~The memory cell in claim 53,~~ A memory cell, comprising:

a transistor;

a capacitor;

a silicon plug extending from said transistor toward said capacitor and physically separate from said capacitor;

a diffusion barrier between said silicon plug and said capacitor, wherein said diffusion barrier is made of a metal nitride, and wherein said diffusion barrier is made of titanium nitride;

an un-nitridized layer of titanium between said diffusion barrier and said silicon plug, wherein said un-nitridized layer of titanium is a silicided layer of titanium, and wherein said silicided layer of titanium is generally as thick as said diffusion barrier.

55. (Original) An interface between a poly plug and a storage node of a capacitor, comprising:

an electrical contact enhancement layer over said poly plug;

a silicon barrier over said electrical contact enhancement layer; and

an oxidation protection layer over said silicon barrier and contacting said storage node.

56. (Original) The interface in claim 55, wherein said electrical contact enhancement layer is a metal silicide layer; said silicon barrier is a metal nitride layer; and said oxidation protection layer is a layer selected from metals, metal oxides, and metal alloys including platinum.

57. (Original) The interface in claim 56, wherein said electrical contact enhancement layer and said silicon barrier contain the same metal.

58. (Original) The interface in claim 56, wherein said electrical contact enhancement layer is of a form $TiSi_X$; and said silicon barrier is made of tungsten nitride.

59. (Original) A part of a semiconductor circuit including insulation over an electrically conductive surface, wherein said insulation defines an opening and a hole from said opening to said surface, wherein said part comprises:

a conductive material filling about half of said hole in said insulation, wherein said conductive material contacts said surface; and

a diffusion barrier at least within said hole and over said conductive material.

60. (Original) The part in claim 59, wherein said diffusion barrier lines said opening.

61. (Original) The part in claim 60, further comprising an oxygen barrier conformal to said diffusion barrier.

62. (Original) A portion of a semiconductor device having an electrically conductive first element, an electrically conductive second element contacting said first element, and an electrically conductive third element configured to electrically communicate with said first element through said second element, wherein said portion comprises:

an oxidation barrier contacting said third element; and

a silicon diffusion barrier contacting said oxidation barrier and said second element;

wherein said oxidation barrier and said silicon diffusion barrier are configured to act as an electrical communication interface between said second element and said third element.

63. (Original) The portion in claim 62, wherein said oxidation barrier and said silicon diffusion barrier define a continuous iridium layer.

64. (Original) The portion in claim 62, wherein said oxidation barrier is made of ruthenium oxide; and said silicon diffusion barrier is also made of ruthenium oxide.

65. (Original) The portion in claim 64, wherein said oxidation barrier and said silicon diffusion barrier define a continuous ruthenium oxide layer.

66. (Currently amended) An interconnect structure, comprising:

a doped polysilicon material having a shape defined by an underlying support structure and an adjacent insulative material;

an electrically conductive material over said doped polysilicon material and said insulative material; and

a silicon barrier between said doped polysilicon material and said electrically conductive material, wherein said silicon barrier contacts said electrically conductive material.

67. (Currently amended) The structure in claim 66, wherein said silicon barrier contacts said doped polysilicon material ~~and said electrically conductive material~~.

68. (Currently amended) ~~The structure in claim 66, further comprising~~ An interconnect structure, comprising:

a doped polysilicon material having a shape defined by an underlying support structure and an adjacent insulative material;

an electrically conductive material over said doped polysilicon material and said insulative material;

a silicon barrier between said doped polysilicon material and said electrically conductive material; and

an oxidation protection layer contacting and interposed between said silicon barrier and said electrically conductive material.

69. (Original) The structure in claim 68, further comprising an electrical contact enhancement layer contacting and interposed between said silicon barrier and said doped polysilicon material.

70. (Currently amended) An interface for a semiconductor device including a poly plug contacting a substrate and a capacitor ~~plate~~ over said poly plug, comprising:

a diffusion barrier under said capacitor ~~plate~~, distal from said capacitor, and over said poly plug, said diffusion barrier selected from a group consisting of:

titanium nitride,

tungsten nitride,

rhenium,

rhenium nitride,

a platinum-group metal,

a nitride of said platinum-group metal~~.~~,

an oxide of said platinum-group metal,

an alloy of said platinum-group metal,

a boride of a transition metal, and

combinations of the above materials.

71. (Currently amended) ~~The interface in claim 70, further comprising~~ An interface for a semiconductor device including a poly plug contacting a substrate and a capacitor over said poly plug, comprising:

a diffusion barrier under said capacitor and over said poly plug, said diffusion barrier selected from a group consisting of: titanium nitride, tungsten nitride, rhenium, rhenium nitride, a platinum-group metal, a nitride of said platinum-group metal, an oxide of said platinum-group metal, an alloy of said platinum-group metal, a boride of a transition metal, and combinations of the above materials; and

an oxidation barrier under said capacitor, over said diffusion barrier, and ~~comprising~~ consisting of a selection of a platinum-group metal and an oxide of said platinum-group metal.

72. (Original) The interface in claim 71, further comprising an electrical contact enhancement layer under said diffusion barrier and over said poly plug, comprising a silicide material.

REMARKS

Claims 1-27 and 29-72 are pending.

Claims 11, 20, 23, 25, 27, 29-31, 34, 36, 39, 43, 45, 48-49, 52-54, 66-68, and 70-71 are amended.

In the interest of efficient prosecution, Applicants note that these claims were rejected during prosecution of the parent application (ser. no. 09/146,108) in an Office Action dated 3/15/00. (A copy of the parent's Office Action dated 3/15/00 is included in an appendix to this Preliminary Amendment.) Applicants cancelled those claims in the parent in the interest of pursuing claim 28. Applicants herein re-present those claims and respond to each basis for rejection separately below.

I. Objection to title

The Examiner announced that the title is not descriptive and required a new title indicative of the invention to which the claims are directed. Applicants have amended the title to -- AN INTERFACE AND METHOD OF FORMING AN INTERFACE FOR A SEMICONDUCTOR DEVICE. Such a title invokes express language from several pending claims, including the "interface" terminology used in claims 16-24, 55-58, and 70-72; the "semiconductor device" terminology used in claims 12-15, 36-42, 62-65; and the "semiconductor" terminology used in claims 5-11, 25-27, 29-35, 59-61. The title also has the benefit of acknowledging both the method claims (1-27, 29-48) as well as the device claims (49-72) within the scope of the invention.

II. Rejection of claims under 35 U.S.C. §112

The Examiner also objected to the Specification and rejected claim 11 based on 35 U.S.C. §112 ¶1. The rejection stems from claim 11's dependence on claim 9. Accordingly, Applicants have amended claim 11 so that it is dependent upon claim 8. (Applicants also note that the Examiner's interpretation of claim 9 does not exactly track that claim's express language. Applicants stress that the claims are limited only by their express language.

Applicants should not be understood to be acquiescing to Examiner statements that do not exactly track any claim's express limitations.) Applicants further note that this §112 rejection is the sole basis for rejecting this claim. Hence, Applicants contend that the amendment results in claim 11 containing allowable subject matter.

The Examiner rejected claim 48 based on 35 U.S.C. §112 ¶2, arguing that antecedent basis is lacking somewhere in the phrase "with a portion of said silicon contact containing oxygen" of that claim. Applicants have clarified that phrase to require "a portion of said silicon contact containing at least one oxygen atom." Applicants further note that this §112 rejection is the sole basis for rejecting this claim. Hence, Applicants contend that the amendment results in claim 48 containing allowable subject matter.

The Examiner rejected claim 71 based on 35 U.S.C. §112 ¶2, arguing that there is no antecedent basis for that claim's use of the term "capacitor." Applicants have amended claim 71 to provide that basis.

III. Rejection of claims under 35 U.S.C. §102

The Examiner rejected several claims under 35 U.S.C. §102, citing one of two references. Applicants address each basis for rejection separately below.

A. Rejection of claims based on U.S. Patent No. 5,506,166

The Examiner rejected claims 20-24, 29-33, 36-38, 43-47, 49-53, 55-57, 59-62, 64, and 66-72 as being anticipated by U.S. Patent No. 5,506,166 (hereinafter '166). Applicants contend that the claims contain limitations distinguishable from '166.

1. Claims 20-24

Claim 20 addresses a method of interfacing a silicon contact with a semiconductor device. In citing '166's disclosure, the Examiner specifically analogized '166's element 65 to claim 20's silicon contact. (Office Action at p. 4.) Significantly, the Examiner failed to express an analogy to claim 20's semiconductor device. (***Id.***) A careful reading suggests that '166

addresses interfacing a polysilicon plug (65) with a capacitor. ('166 at Abstract; Summary.) Thus, the rejection carries an implicit analogy between claim 20's semiconductor device and '166's elements 95, 90, and 85 (and possibly elements 75 and 65 as well – *see* '166 at col. 6, ln. 50-56). Claim 20's method requires forming a barrier to oxidation; and the Examiner cited the formation of '166's bottom capacitor plate 85 against that claimed act. (Office Action at p. 4.) However, claim 20 has been clarified to indicate that the barrier to oxidation is discrete from the semiconductor device mentioned in the preamble. This is in direct contrast to '166's capacitor plate 85, which is an integral part of the relevant semiconductor device in '166 – the capacitor made of at least elements 85, 90, and 95. Thus, because the Examiner's citation discloses only the exact opposite of the relevant claim limitation, the §102 rejection against claim 20 fails. Dependent claims 21-24 benefit accordingly.

2. Claims 29-33

Claim 29 has been clarified to require an act of selectively depositing a material over doped polysilicon. The Examiner has analogized '166's polysilicon plug 65 to claim 29's doped polysilicon. (Office Action at p. 5.) However, no excerpt from '166 appears to disclose selectively depositing a material over '166's polysilicon plug 65. Rather, '166 discloses only non-selective depositions thereover. ('166 element 66, FIG. 7; element 75, FIGS. 9A&B; element 85, FIGS. 11A&B; element 90, FIGS. 13A&B; element 95, FIGS. 13A&B.) Because '166 discloses only the exact opposite of the relevant claim limitation, the §102 rejection against claim 29 fails. Dependent claims 30-33 benefit accordingly.

3. Claims 36-38

Claim 36 has been clarified to require an act of selectively providing an initial barrier component on an interconnect material. The Examiner has analogized '166's polysilicon plug 65 to claim 36's doped interconnect material. (Office Action at p. 6.) However, no excerpt from '166 discloses selectively depositing a material on '166's polysilicon plug 65. Rather, '166 discloses only a non-selective deposition thereon. ('166 element 66, FIG. 7.) Because '166

discloses only the exact opposite of the relevant claim limitation, the §102 rejection against claim 36 fails. Dependent claims 37 and 38 benefit accordingly.

4. Claims 43-47

The Examiner initially announced that claims 43-47 were anticipated by '166. (Office Action at p. 4.) However, the subsequent pages contain no application of '166 excerpts to the particular limitations of these claims. (Office Action at p. 4-9.) Accordingly, Applicants contend that the Examiner has failed to meet the *prima facie* burden for rejecting claims 43-47 under this basis.

5. Claims 49-53

Claim 49 has been clarified to require a contact enhancer physically integral to the diffusion barrier. The Examiner has analogized '166's titanium nitride layer 75 to claim 49's diffusion barrier. (Office Action at p. 6.) Applicants contend that no portion of '166 could arguably be characterized as a contact enhancer that is physically integral to'166's titanium nitride layer 75. Rather, such portions of '166 appear to be only physically separate layers. Because '166 discloses only the exact opposite of the relevant claim limitation, the §102 rejection against claim 49 fails. Dependent claims 50-53 benefit accordingly.

6. Claims 55-57

Claim 55 has always required an oxidation protection layer contacting a storage node of a capacitor. In attempting to reject this claim, the Examiner sought to analogize '166's element 85 to claim 55's oxidation protection layer. (Office Action at p. 7.) However, '166's element 85 *is* the storage node of '166's capacitor. Hence, that element cannot satisfy claim 55's "contacting" requirement. Because '166's storage node cannot reasonably serve as both claim 55's oxidation protection layer as well as claim 55's capacitor storage node, the §102 rejection against claim 55 fails. Dependent claims 56-57 benefit accordingly.

7. Claims 59-61

Claim 59 has always required a conductive material filling "about half" of a hole in insulation. In attempting to reject this claim, the Examiner sought to analogize '166's polysilicon plug 65 to claim 59's conductive material. (Office Action at p. 7.) However, in no figure from '166 is the polysilicon plug 65 illustrated as filling "about half" of any opening 50 in the oxide 40. Rather, the filling is illustrated as being more extensive. (*See* '166 at FIGS. 6-13B.) As for '166's text, it merely discloses that its oxide 40 is "thick" (***id.*** at col. 4, ln. 38) and that the polysilicon plug 65 is etched back 50-400 nm (***id.*** at col. 5, ln. 22-23). Applicants contend that such textual disclosure is insufficient to disclose claim 59's "about half" limitation, especially when '166's text is considered in light of '166's figures. Applicants contend that the Examiner's reliance on '166's cited excerpts represents a failure to meet the burden for rejecting claim 59 and its dependent claims 60-61.

8. Claims 62 and 64

Claim 62 has always required an oxidation barrier contacting an electrically conductive "third element" addressed in the preamble. In attempting to reject this claim, the Examiner sought to analogize '166's bottom capacitor plate 85 to claim 62's oxidation barrier and further sought to analogize '166's top capacitor plate 95 to claim 62's "third element." (Office Action dated 3/15/00 at p. 8.) However, '166's bottom capacitor plate 85 and top capacitor plate 95 do not contact each other. Rather, they are separated by dielectric 90. Hence, '166 fails to disclose claim 62's contacting requirement.

The rejection contains another failed analogy that further defeats anticipation by '166. Claim 62 has always required a silicon diffusion barrier contacting an electrically conductive "second element" addressed in the preamble. The Examiner sought to analogize '166's titanium nitride layer 75 to claim 62's silicon diffusion barrier and further sought to analogize 166's polysilicon plug 65 to claim 62's "second element." (Office Action dated 3/15/00 at p. 8.) However, '166's titanium nitride layer 75 and polysilicon plug 65 do not contact each other. Rather, they are separated by titanium silicide 67. Hence, '166 fails to disclose another contacting requirement of claim 62.

Because the Examiner's citation to '166 discloses only the exact opposite of the claim 62's contacting requirements, the §102 rejection against claim 62 fails. Dependent claim 64 benefits accordingly.

9. Claims 66-69

Claim 66 now express a limitation formerly expressed in dependent claim 67. Specifically, claim 66 requires a silicon barrier that contacts an electrically conductive material. The Examiner sought to analogize '166's titanium nitride layer 75 to claim 66's silicon barrier and further sought to analogize '166's top capacitor plate 95 to claim 66's electrically conductive material. (Office Action at p. 8.) However, '166's titanium nitride layer 75 and top capacitor plate 95 do not contact each other. Rather, they are separated by the bottom capacitor plate 85 and dielectric 90. Hence, the Examiner's citations to '166 fail to disclose the contact requirement of claim 66 and in fact disclose only the opposite. As a result, the §102 rejection against claim 66 fails. Dependent claim 67 benefits accordingly.

Claim 68 has always required an oxidation protection layer contacting claim 66's electrically conductive material. The Examiner sought to analogize '166's bottom capacitor plate 85 to claim 68's oxidation protection layer. (Office Action at p. 9.) As mentioned above, the Examiner sought to analogize '166's top capacitor plate 95 to the electrically conductive material. However, '166's bottom capacitor plate 85 and top capacitor plate 95 do not contact each other. Rather, they are separated by dielectric 90. Hence, the Examiner's citations to '166 fail to disclose claim 68's contacting requirement and in fact disclose only the opposite. Accordingly, the only amendment to claim 68 has been to place it in independent form by expressing the limitations originally presented in claim 66. Dependent claim 69 benefits from the failure of '166's cited excerpt to disclose this "contacting" limitation as well.

10. Claims 70-72

Claim 70 has been clarified to require that its diffusion barrier be distal from the capacitor mentioned in the preamble. The Examiner sought to analogize '166's titanium nitride layer 75 to claim 70's diffusion barrier. (Office Action at p. 9.) However, '166's titanium nitride

layer 75 is not distal from '166's capacitor. Rather, '166's titanium nitride layer 75 is directly adjacent to '166's capacitor. Having disclosed only the exact opposite of the claim 70 clarification, the Examiner's citation to '166 cannot be interpreted as anticipating that claim.

Claim 71 has always required an oxidation barrier under the capacitor. The Examiner sought to analogize '166's bottom capacitor plate 85 to claim 71's oxidation barrier. (Office Action at p. 9.) However, because '166's element 85 is a part of the capacitor, it cannot be understood to be under the capacitor. Therefore, the Examiner's analogy fails to meet that claim limitation, and '166 cannot be understood to be anticipate claim 71. Dependent claim 72 benefits accordingly.

B. Rejection of claims based on U.S. Patent No. 5,504,041

The Examiner rejected claims 43-47 as being anticipated by a patent by Summerfelt, presumably U.S. Patent No. 5,504,041 (hereinafter '041). (Office Action at p. 10.) Applicants contend that the claims contain limitations distinguishable from '041. Claim 43, for instance, has been clarified to require an act of depositing a barrier component "selectively" onto the silicon contact. Nowhere in the Examiner's citation of '041 -- column 9, lines 18-28 of '041 -- is depositing selectively disclosed. Rather, that excerpt discloses a non-selective sputter deposition, with a selective chemical removal thereafter. Because the Examiner's citation discloses only the exact opposite of the relevant claim limitation, that citation necessarily fails to anticipate claim 43. Dependent claim 44 benefits accordingly.

Claim 45 has always required an act of *discretely* siliciding the barrier component in addition to nitridizing the barrier component. This is in contrast to the excerpt cited by the Examiner, wherein an anneal in a nitrogen-containing atmosphere integrates both siliciding and nitridizing '041's titanium. Thus, the Examiner's citation discloses only the exact opposite of the relevant claim limitation and cannot be read to anticipate claim 45. Dependent claims 46-47 benefit accordingly. As a result, claim 45 has been amended to independent form by expressing only the original limitations expressed in claim 43. Moreover, dependent claim 46 further details the act of discretely siliciding and is therefore even further distinguished from '041's relevant excerpt. Dependent claim 47 benefits from that distinction as well. In addition, dependent claim

47 still further details the act of discretely siliciding and is therefore yet further distinguished from '041's relevant excerpt.

IV. Rejection of claims under 35 U.S.C. §103

The Examiner rejected several claims under 35 U.S.C. §103, citing several prior art combinations. Applicants address each combination separately below.

A. Rejection of claims based on '166 in combination with the Examiner's unsupported conclusion concerning routine skill in the art

The Examiner rejected claims 54, 58, and 65 as being obvious, citing '166 as a partial basis for the rejection. The Examiner acknowledged that '166 fails to disclose every limitation of the rejected claims and attempted to cure '166's lack of disclosure with bare conclusions concerning routine skill in the art. Applicants address each claim separately below.

1. Claim 54

Claim 54 has always required a silicided layer of titanium that is generally as thick the diffusion barrier included as part of the claimed memory cell. The Examiner indicated that '166 did not disclose such a limitation. Nevertheless, the Examiner announced (without citation to authority) that the optimum or workable ranges of the thickness of any layer involves routine skill in the art. (Office Action at p. 11.) The Examiner concluded that, merely because the claim expresses a dimension limitation, it is Applicants' burden to show the critical nature of that dimension or an unexpected result therefrom. (***Id.***) However, MPEP §2144.05 II(B) demonstrates that the Examiner's bare conclusion has failed to meet the *prima facie* burden for rejecting this claim. Specifically, that section of the MPEP requires that, before labeling the variable at issue as an optimization, prior art must recognize that the variable achieves a recognized result. The case precedent cited therein indicates that it is the Examiner's burden to establish that prior art recognition. (*See id.* (citing ***In re Antonie***, 559 F.2d 618, 195 U.S.P.Q. 6 (C.C.P.A. 1977)). A copy of the MPEP and this case is included in an appendices to this

Preliminary Amendment.) The Examiner, unfortunately, made no such effort to establish what is recognized in the prior art concerning the thickness of claim 54's silicided layer of titanium in relation to that of the diffusion barrier. Instead, the Examiner merely designated that limit as an optimization in a conclusory manner, thereby contradicting the MPEP and ***Antonie***.

The Examiner's statements concerning routine skill in the art face similar problems in terms of their contradiction with other binding case precedent. In ***In re Zurko*** (258 F.3d 1379, 59 U.S.P.Q.2d 1693 (Fed. Cir. 2001), the Patent and Trademark Office (PTO) rejected Zurko's claims based on the PTO's assumptions concerning the technology. (*See* ***id.***, 59 U.S.P.Q.2d at 1695. A copy of ***Zurko*** is included in an appendix to this Preliminary Amendment.) The Court reversed the PTO, indicating that, with respect to "core factual findings in a determination of patentability," the PTO "cannot simply reach conclusions based on its own understanding or experience -- or on its assessment of what would be basic knowledge or common sense." (***Id.*** at 1697.) Rather, the Court required the PTO to "point to some concrete evidence in the record" in support of its findings. (***Id.***) The Court reasoned that to hold otherwise would render the process of appellate review a meaningless exercise. (***Id.***) The current facts are analogous: the Examiner has been unwilling or unable to cite prior art disclosing the thickness of claim 54's silicided layer of titanium in relation to its diffusion barrier. Absent such disclosure, the Examiner must necessarily be relying on assumptions concerning the technology, reaching conclusions based on the Examiner's own understanding or experience -- or on an assessment of what would be basic knowledge or common sense. Applicants contend such conduct is an invitation for reversal by the Board or the Court for the same reasons as those provided in ***Zurko***. Applicants request that the Examiner avoid such reversal by withdrawing this rejection.

More generally, the Examiner's attempt to address substantive express claim limitations merely by announcing a rule contradicts the admonitions of the Board and Court against avoiding substantive analysis of the limitations by mechanically applying a rule. For example, in ***Ex parte Ohrnberger*** (1996 WL 1749366 (Bd. Pat. App. & Interf. 1996)) the Examiner rejected the claims as being obvious, relying on ***In re Karlson*** (311 F.2d 581, 136 U.S.P.Q. 184 (C.C.P.A. 1963)) for the proposition that it is routine skill in the art to omit an element and its function in a combination where the remaining elements perform the same functions as before. In reversing the Examiner, the Board recognized that the Court has held that ***Karlson***'s rule is not a mechanical rule, and that ***Karlson*** is not intended to short circuit the determination of

obviousness mandated by 35 U.S.C. §103. (***Ohrnberger***, 1996 WL 1749366 at 3 (citing ***In re Wright***, 343 F.2d 761,769-70, 145 U.S.P.Q. 182, 190 (C.C.P.A. 1965)). Copies of ***Ohrnberger, Karlson,*** and ***Wright*** are included in appendices to this Preliminary Amendment.) Accordingly, the ***Ohrnberger*** Board conducted a substantive analysis of the limitations, the prior art, and the obviousness standard (as did the ***Wright*** Court) and found the Examiner failed to meet the *prima facie* burden. (***Ohrnberger***, 1996 WL 1749366 at 3; *see also* ***Wright*** at 145 U.S.P.Q. at 190.) Applicants contend that the Examiner's mere announcements that (1) the optimum or workable ranges of the thickness of any layer involves routine skill in the art and (2) a claim limitation based on dimensions automatically shifts the burden to Applicants to show criticality or unexpected results represent the very circumstances the Board and Court seek to avoid – a mechanical application of a rule that circumvents the determination of obviousness mandated by 35 U.S.C. §103.

The rejection's contradiction to binding case precedent demonstrates that the Examiner has failed to meet the *prima facie* burden for rejection. Accordingly, the only amendment to claim 54 has been to place it in independent form, expressly incorporating the limitations originally presented in claims 49-53.

2. Claim 58

Claim 58 has always required a silicon barrier made of tungsten nitride. The Examiner admits that '166 does not specify that. (Office Action at p. 11.) Nevertheless, having previously analogized 166's layer 75 to the claimed silicon barrier (Office Action at p. 7), the Examiner indicated that layer 75 could be a metal nitride. (*See* Office Action at p. 11.) As support for 166's layer being made of this material, the Examiner cited '166's column 5, lines 25-47. However, that excerpt does not address the materials for '166's element 75. Rather, it addresses '166's layer 67. Accordingly, the Examiner has failed to cite adequate support for the rejection.

A second problem with the rejection is highlighted by the Examiner's attempt to make up for '166's lack of relevant disclosure. Specifically, the Examiner once again issued conclusions about what is routine skill and what is well known in the art. (Office Action at p. 11.) In doing so, the Examiner has once again contradicted the binding case precedent of ***Zurko*** (59

U.S.P.Q.2d 1693); ***Ohrnberger*** (1996 WL 1749366 at 3); and ***Wright*** (145 U.S.P.Q. at 190); as detailed above in part 1.

The third problem with the rejection is that dependent claim 58 incorporates the limits of independent claim 55. As discussed above in part III(A)(6), such limits include the "contacting" requirement that '166 fails to disclose. Claim 58 benefits from that distinction, and the Examiner's obviousness analysis does not cure that lack of disclosure. Thus, for any one or combination of reasons discussed above, the Examiner has failed to satisfy the *prima facie* burden for rejecting claim 58.

3. Claim 65

Claim 65 requires that the oxidation barrier and silicon diffusion barrier define a continuous ruthenium oxide layer. The Examiner concluded that it would be obvious to form '166's ruthenium oxide bottom capacitor plate 85 and ruthenium oxide layer 75 from a continuous layer of ruthenium oxide. (Office Action at p. 12.) Support for this conclusion stems from the Examiner's announcement concerning routine skill in the art. (***Id.***) Once again, the Examiner's announcement contains no citation to case precedent, thereby denying Applicants a full and fair opportunity to respond, such as by distinguishing the case relied upon. In addition, the Examiner's announcement appears to be nothing more than a mechanical application of a rule in order to avoid substantive obviousness analysis. As a result, the Examiner's mechanical rule application is legally improper in light of case precedent. (*See* ***Ohrnberger***, 1996 WL 1749366 at 3; ***Wright***, 145 U.S.P.Q. at 190.) Moreover, the Examiner's announcement lacks citation to concrete evidence concerning the relevant technology and instead appears to be based on the Examiner's own understanding, experience, or assessment of what would be basic knowledge or common sense. As a result, the Examiner's baseless opinion is legally improper in light of still other binding case precedent. (*See* ***Zurko***, 59 U.S.P.Q.2d at 1697.)

Still another problem with the rejection is that dependent claim 65 incorporates the limits of independent claim 62. As discussed above in part III(A)(8), such limits include the "contacting" requirements that '166 fails to disclose. Claim 65 benefits from that distinction, and the Examiner's obviousness analysis does not cure that lack of disclosure. Thus, for any one

or combination of reasons discussed above, the Examiner has failed to satisfy the *prima facie* burden for rejecting claim 65.

B. Rejection of claims based on '166 in combination with '041

The Examiner rejected claims 1-8, 12-15, 39-42, and 63 as obvious in light of '166 in combination with '041. However, an obviousness rejection requires that the multiple prior art references suggest to one of ordinary skill in the art to combine the references. (*See* ***United States Surgical Corp. v. Ethicon Inc.***, 103 F.3d 1554, 1564, 41 U.S.P.Q.2d 1225, 1233 (Fed. Cir. 1997), *cert. denied*, 522 U.S. 950 (1997).) Further, when the prior art contains conflicting references, the inability of each reference to suggest solutions to one of ordinary skill in the art must be considered. (*See* ***In re Young***, 927 F.2d 588, 18 U.S.P.Q.2d 1089, 1091 (Fed. Cir. 1991).) Specifically, the Examiner must consider whether one reference discredits another. (***Id.*** Copies of these cases are included in appendices to this Preliminary Amendment.) Applicants contend that such consideration reveals that '166 and '041 conflict with each other so greatly that they are unable to suggest solutions that cover the limitations in the pending claims to one of ordinary skill in the art.

The embodiments emphasized in '166, for example, concern a platinum electrode on a titanium nitride layer, which is in turn over a titanium silicide layer, wherein the titanium silicide is over a polysilicon plug. The embodiment in '041 predominantly relied upon by the Examiner for the rejections has a similar arrangement of materials. (*See* Office Action at p. 13 (citing '041 at col. 9, ln. 18-28).) Significantly, however, '041 emphasizes providing a barrier 34 between its platinum electrode and titanium nitride layer. ('041 at col. 9, ln. 18-28.) The teachings in '041 emphasizing that barrier 34 highlight many of the conflicts between the references. Specifically, '041 warns that the platinum electrode will allow oxygen to diffuse therethrough and oxidize underlying the titanium nitride. ('041 at col. 2, ln. 52-64; col. 5, ln. 52-62.) In fact, '041 repeatedly warns ordinary artisans about how relatively quickly titanium nitride oxidizes. (***Id.*** at col. 4, ln. 60-62; col. 5, ln. 34-36; col. 6, ln. 17-19; col. 9, ln. 8-10.) The '041 reference specifies that the dangers of oxidizing titanium nitride include the expansion of that layer's size as well as increased contact resistance. (***Id.*** at col. 5, ln. 52-66.) Such teachings, however, are in direct contradiction to those in '166, which indicates that the platinum electrode protects materials in

general and the titanium nitride in particular from oxidation. ('166 at col. 2, ln. 14-16; col. 6, ln. 18-19; col. 7, ln. 10-15.) Thus, one of ordinary skill in the art keeping '041 in mind would view '166 as being discredited in its teachings concerning the ability of platinum to protect against oxidation. Such an artisan continuing to keep in mind '041 in mind would further view '166 as inviting oxidation of the titanium nitride layer, which in turn would lead to undesirable results such as volume expansion and high contact resistance. Conversely, one of ordinary skill in the art keeping '166 in mind would view '041 as being discredited in its teachings concerning the platinum's tendency to allow oxidation. Such an artisan continuing to keep in mind '166 in mind would further view '041 as requiring unnecessary process time, expense, and complexity in providing a barrier layer that is redundant in light of the existing titanium nitride layer.

The choice of electrode material raises another conflict between the references. As an alternative to platinum, '166 emphasizes ruthenium oxide. ('166 at col. 6, ln. 31-34; claim 19.) While '041 addresses ruthenium oxide as one of a legion of alternatives to platinum ('041 at Table 1), '041 nevertheless warns ordinary artisans that ruthenium oxide is considered to be "inferior" and allows for leakage current that is undesirably "several orders of magnitude" larger than embodiments using platinum (***id.*** at col. 2, ln. 65-col. 3, ln. 12). Thus, one of ordinary skill in the art keeping '166 in mind would view '041 as unnecessarily discouraging a viable alternative to a platinum electrode. Conversely, one of ordinary skill in the art keeping '041 in mind would view '166 as encouraging ordinary artisans to use an inferior material that undesirably causes an enormous amount of leakage current.

Each reference's treatment and location of its barrier illustrate yet another conflict. Elements 1 and 75 of '166 are identified as barriers, and '166 alerts artisans of the dangers of allowing that barrier to oxidize. Specifically, '166 warns that, because barrier 1 is over the opening defined by the supporting oxide, the exposed sides of barrier 1 will oxidize which, in turn, will cause the polysilicon plug 3 to oxidize. ('166 at col. 2, ln. 20-24.) As a result, capacitance will be decreased and density goals will be frustrated. (***Id.*** at ln. 24-28.) To avoid such problems, '166 teaches locating its barrier 75 within an opening defined by the oxide, thereby protecting the barrier's sides. (***Id.*** at col. 2, ln. 54-55; col. 3, ln. 15-20; col. 6, ln. 5-14; col. 7, ln. 10-14; FIGS 10A&B.) In direct contrast, many of the embodiments illustrated and discussed in '041 place the barrier 34 over the opening defined by supporting oxide 32. ('041 at FIGS. 8-9, 11-16.) Further, in at least one embodiment, '041 actively encourages oxidizing at

least the sides of its barrier. (***Id***. at col. 10, ln. 11-12; FIGS. 13-15.) In alternative embodiments, '041's entire barrier is already oxidized. (***Id***. at ln. 12-14.) '041 suggests that such oxidation actually protects the underlying layers from oxidation. (*See* ***id***. at col. 10, ln. 19-27.) Thus, one of ordinary skill in the art keeping '166 in mind would view '041 as unduly risking oxidation of conductive elements under the barrier, thereby undesirably decreasing capacitance and frustrating density efforts. Conversely, one of ordinary skill in the art keeping '041 in mind would view '166's oxidized barriers as unduly risking oxidation of underlying conductive elements. Such an artisan continuing to keep '041 in mind would further view '166 as requiring unnecessary time, money, effort, and process complexity in restricting the barrier to within an opening in insulation.

Even when the references describe analogous layers, their teachings highlight still other contradictions. As mentioned above, both references address embodiments concerning titanium nitride over titanium silicide, which, in turn, is over polysilicon. ('041 at col. 9, ln. 18-28, FIG. 9; '166 at col. 5, ln. 26-52, FIGS. 10A&B.) '166 teaches a process that first provides titanium silicide and may also provide titanium nitride as well. ('166 at col. 5, ln. 26-42.) However, '166 also teaches removing all nitride, then providing a discrete second layer of titanium nitride. (***Id***. at ln. 43-52.) '041 teaches a process that expressly provides titanium silicide as well as titanium nitride as well. ('041 at col. 9, ln. 18-27.) In contrary to '166's teachings, '041 emphasizes retaining at least some of the titanium nitride. (***Id***. at ln. 27-28.) As a result, one of ordinary skill in the art keeping '166 in mind would view '041 as retaining undesirable nitride. Conversely, one of ordinary skill in the art keeping '041 in mind would view as'166 as requiring unnecessary cost, time, effort, and process complexity by requiring the removal of a material followed by subsequently re-providing that material.

Applicants contend that any one or combination of the conflicts addressed above – ranging from the very excerpts relied upon by the Examiner to the teachings as a whole –actively discourage an ordinary artisan from combining the references. Thus, without comment on the claims and without acquiescing to the Examiner's interpretation of the limitations, Applicants contend that such discouragement demonstrates the improper hindsight used in attempting to articulate a motive to combine. Such discouragement also demonstrates the general failure to meet the *prima facie* burden for rejecting claims based on a combination of '041 and '166.

Moreover, dependent claim 63 benefits from the misapplication of '166 against independent claim 62, as addressed above in part III(A)(8). As the Examiner has not explained how adding '041's disclosure cures that misapplication, such a failure provides yet another indication that the *prima facie* burden for rejecting claim 63 has not been met.

C. Rejection of claims based on '166 in combination with '041 and U.S. Pat. No. 5,173,327

The Examiner rejected claims 9-10 and 16-19 as obvious in light of '166 in combination with '041 and U.S. Pat. No. 5,173,327 (hereinafter '327). However, as discussed above in part B, the conflicts between '166 and '041 actively discourage an ordinary artisan from combining the references, and the Examiner has not articulated how adding '327 cures such contradictions. In addition, Applicants contend that the Examiner has misinterpreted the teachings of '327. Applicants note that the Examiner announced that '327 teaches selective deposition, citing the entirety of '327's "Detailed Description" section. (Office Action at p. 20, 22.) Applicants contend that a careful reading of '327 does not reveal disclosure of selective deposition. Applicants submit that any one or combinations of the '166/'041 conflicts and '327 misinterpretation demonstrate the Examiner's failure to satisfy the *prima facie* burden for rejecting these claims.

D. Rejection of claims based on '041 in combination with the Examiner's unsupported conclusion concerning well known techniques

The Examiner rejected claims 25-26 as obvious in light of '041 in combination with techniques that the Examiner deems, without citation, to be well known. (Office Action at p. 23.) Such unsupported conclusions by the Examiner yet again contradicts the binding case precedent of ***Zurko*** (59 U.S.P.Q.2d 1693); ***Ohrnberger*** (1996 WL 1749366 at 3); and ***Wright*** (145 U.S.P.Q. at 190); as detailed above in part IV(A)(1). Such binding case precedent demonstrates the impropriety of the Examiner's baseless announcement concerning well known techniques in the art and therefore the failure to meet the *prima facie* burden for rejecting claims 25-26 as being obvious.

In addition, claim 25 has been clarified to require an act of "selectively" depositing at least one metal layer within the hole over the doped polycrystalline silicon. Nowhere in the Examiner's citation of '041 -- column 9, lines 18-28 -- is depositing selectively disclosed. Rather, that excerpt discloses a non-selective sputter deposition, with a selective chemical removal thereafter. Because the Examiner's citation discloses only the exact opposite of the relevant claim limitation, that citation necessarily teaches away from the relevant limitation in claim 25. Further, the Examiner's assumption of what techniques are well known, assuming *arguendo* it could be supported by concrete evidence, does not address the "selectivity" limitation. Hence, given '041's citation teaching away and the Examiner's assumption's silence on this matter, the combination of the two still teaches away and thereby supports non-obviousness. Dependent claim 26 benefits accordingly.

E. Rejection of claim based on '041 in combination with '166

The Examiner rejected claim 27 as obvious in light of '041 in combination with '166. Applicants contend that there are flaws in the Examiner's rejection. For example, the Examiner goes so far as to admit that the '041 excerpt relied upon fails to disclose nitridizing a non-titanium layer. (Office Action at p. 24.) Applicants submit that the Examiner's excerpt goes even farther by actively teaching the exact opposite – nitridizing a titanium layer. ('041 at col. 9, ln. 25-27.) Applicants contend that the Examiner's down-playing of the teachings in the very '041 excerpt relied upon by the Examiner represents a misapplication of that reference. Such a misapplication demonstrates the failure to meet the *prima facie* burden for rejection.

Still other indications of this failure can be found in the instances wherein '041 and '166 contradict each other, as detailed above in part IV(B). Such contradictions demonstrate that the references, when viewed as a whole, discredit each other and fail to suggest solutions to one of ordinary skill in the art. In fact, such contradictions actively discourage combination.

Yet another indication of the failure to meet the *prima facie* burden for rejection can be found in the Examiner's attempt to apply '166 and articulate the motive for combining the references. The Examiner addressed the nitridizing of '166's non-titanium layer by merely announcing that it is "within the level of ordinary skill in the art." (Office Action at p. 24.) As with similar conclusions from the Examiner addressed above, such unsupported conclusions

contradict the binding case precedent of ***Zurko*** (59 U.S.P.Q.2d 1693); ***Ohrnberger*** (1996 WL 1749366 at 3); and ***Wright*** (145 U.S.P.Q. at 190). (*See* above, part IV(A)(1).)

Applicants contend that any one or combination of these failures demonstrate the failure to meet the *prima facie* burden for rejecting claim 27. Accordingly, the only amendment to that claim has been to place it in independent form, expressly incorporating the original limitations of claim 25.

F. Rejection of claims based on '166 in combination with the Specification's prior art

The Examiner rejected claims 34 and 35 as being obvious in light of '166 in combination with prior art addressed in the Specification. However, as addressed above, an obviousness rejection requires that the multiple prior art references suggest to one of ordinary skill in the art to combine the references. (*See* ***Ethicon Inc.***, 41 U.S.P.Q.2d at 1233.) Further, when the prior art contains conflicting references, the inability of each reference to suggest solutions to one of ordinary skill in the art must be considered, including one reference discrediting the other. (*See* ***Young***, 18 U.S.P.Q.2d at 1091.) Applicants contend that such consideration reveals that '166 and the Specification's prior art conflict with each other so greatly that they are unable to suggest solutions that cover the limitations in the pending claims to one of ordinary skill in the art.

For example, it is significant that the prior art addressed in the Specification illustrates direct contact between the poly plug 28 and the bottom plate 34 of capacitor 40. (*See* Specification at figure 2.) This is in direct contrast to '166's teachings, which tout providing a plurality of layers between the polysilicon plug and bottom capacitor plate in order to provide low contact resistance and to prevent diffusion of various materials. ('166 at col. 2, ln. 6-14, 62-64; col. 5, ln. 43-48; col. 6, ln. 5-14; FIGS. 13A, 13B.) Thus, one of ordinary skill in the art keeping in mind the Specification's prior art would view '166 as requiring unnecessary time, money, effort, and process complexity for device fabrication. Conversely, such an artisan keeping in mind '166 would view the Specification's prior art as undesirably allowing high contact resistance as well as allowing materials to diffuse throughout the devices being fabricated. Such contradictory teachings actively discourage one of ordinary skill in the art from combining the teachings of '166 with those in the Specification's prior art.

Further, even if an ordinary artisan would be motivated to ignore that conflict, additional conflicts arise that would further discourage combining these references. In particular, it is noteworthy that the prior art addressed in the Specification favors a poly plug that fully extends through the surrounding insulation 32. Thus, assuming *arguendo* that an ordinary artisan would be motivated to place a barrier layer over the poly plug 28 of the Specification's prior art, the artisan would achieve the structure illustrated in '166's Figure 1, which is expressly criticized by '166 as allowing oxidation of the barrier and the polysilicon plug, thereby decreasing capacitance and frustrating attempts to make the memory device denser. ('166 at col. 2, ln. 20-34.) Thus, one of ordinary skill in the art keeping in mind the Specification's prior art would view '166 as requiring unnecessary time, money, effort, and process complexity in controlling the height of the poly plug. Conversely, such an artisan keeping in mind '166 would view the Specification's prior art as undesirably allowing oxidation of the barrier and the polysilicon plug, a decrease in capacitance, and a memory device that takes up too much space. As a result, one of ordinary skill in the art is further actively discouraged from combining the teachings of '166 with those in the Specification's prior art.

The Examiner specifically argues that one of ordinary skill in the art would be motivated to replace '166's planar capacitor formed in the clear with one formed within an opening defined by insulation. (Office Action at p. 26.) The Examiner's proposed motivation is the greater surface area (and therefore greater capacitance) gained by forming the capacitor in the insulation's opening. Significantly, '166 acknowledges the desire to increase capacitance by increasing surface area. ('166 at col. 6, ln. 38-44.) However, '166 achieves this desire in a way that is not necessarily compatible with forming a capacitor in an opening. Specifically, '166 expressly encourages providing a thick bottom electrode so that its sides can contribute to capacitance. (***Id.***) Assuming that such a thick layer can even be provided in a container with sufficient step coverage, such a thick layer risks completely filling the container 26 in the Specification's prior art, thereby leaving no room for the dielectric 36 and top capacitor plate 38, providing no extra capacitance, and defeating the whole point of forming the container in the first place. This risk increases as ordinary artisans strive to meet '166's goal of denser and smaller memory devices. (*See* ***id.*** at col. 1, ln. 32-35.)

Also significant is the fact that '166 acknowledges forming components in an opening defined by insulation. ('166 at FIGS. 4-5.) '166 even allows its capacitor to be partially formed

therein. (***Id.*** at FIGS. 11B, 12B, 13B.) Nevertheless, '166 expressly illustrates the substantially planar nature of its capacitor and expressly touts techniques directed to formation of a capacitor outside of such an opening. (***Id.*** at FIGS. 11A&B, 12 A&B, 13 A&B; col. 6, ln. 15-65.) Applicants contend that '166's touting of a planar capacitor despite acknowledging formation of devices completely within openings defined by insulation would discourage an ordinary artisan from forming '166's capacitor completely in an opening defined by oxide - the very modification suggested by the Examiner.

Thus, the teachings in '166 directed to the surface area issue teach away from the Specification's prior art suggestion based on the same issue. Again without comment on the claims and without acquiescing to the Examiner's interpretation of the limitations, Applicants contend that one of ordinary skill in the art is still further actively discouraged from even attempting to combine the teachings of '166 with those in the Specification's prior art.

Furthermore, at the time of invention, one of ordinary skill in the art was led to believe that the capacitor dielectric material touted by '166 was incompatible with forming a capacitor in an opening defined by insulation. The '166 reference emphasizes the need for providing the high K dielectric using an oxidizing atmosphere. ('166 at col. 1, ln. 60-62.) The '166 reference also emphasizes the need to protect its barrier 75 from that oxidizing atmosphere, and achieves this at least in part by locating the barrier 75 in an opening defined by insulation. (***Id.*** at col. 2, ln. 54-55; col. 3, ln, 15-19; col. 7, ln. 11-14.) The Examiner's proposed modification would involve locating the high K dielectric in an opening defined by insulation. (Office Action dated 3/15/00 at p. 26.) Thus, according to 166's teachings, the dielectric would be at least partially isolated from the oxidizing atmosphere, which is undesirable. Thus, the very reference cited by the Examiner further refutes the Examiner's attempted modification. As a result, one of ordinary skill in the art is still further actively discouraged from combining the teachings of '166 with those in the Specification's prior art.

Any one or combination of the contrary teachings addressed above demonstrate that the conflict between the two references is so great that their ability to suggest solutions is hampered to the point that one of ordinary skill in the art is discouraged from combining them. As a result, the *prima facie* burden for rejecting claims 34 and 35 has not and cannot be met relying on '166's teachings in combination with prior art addressed in the Specification.